

In the United States Patent and Trademark Office

In re the Application of
Lee D. Whetsel

TI-14124D.6

Divisional of Appln No: 10/469,274

Previous Art Unit: 2131

Filed: October 20, 2003

Previous Examiner: Hua, Ly

Title: Digital Bus Monitor Integrated Circuits

**Petition to Make Special
Under 37 CFR 1.102 and
MPEP section 708.02, Paragraph VIII**

October 22, 2003

Asst. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is
being deposited with the U.S. Postal Service as
Express Mail airbill EV33320875US in an envelope
addressed to: Assistant Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450 on
October 22, 2003.

Lawrence J. Bassuk, Reg. No. 29,043

Dear Sir:

Petition With Fee

Applicant submits this petition to make special accompanied
by the fee set forth in 37 CFR 1.17(h).

Please charge the fee under 37 CFR 1.17(h) of \$130.00 to the
deposit account of Texas Instruments Incorporated, Account No.20-
0668.

Claims Directed To Single Invention

The accompanying Preliminary Amendment A presents claims
directed to a single invention.

Statement of Pre-Examination Search Performed

Applicant submits a copy of a pre-examination search report letter, dated September 22, 2003, from an Arlington, Virginia search firm.

Each report letter lists the subject matter of the search, lists the field of search, and states that the subclasses for searching were confirmed by an examiner.

Submission of Most Closely Related References

The search report letter lists the art located in that search.

The electronically filed Information Disclosure Statement A (IDS-A) and accompanying PTO-1449 forms list US patents and US Patent Application Publications located in the pre-examination searches. The electronically filed IDS-A papers also list US patents of the present named inventor, and US patents and US Patent Application Publications cited in corresponding and other patent applications of the present named inventor. Under the new rules, applicant does not submit any copies of the US patents or US Patent Application Publications cited in the electronically filed IDS-A.

An enclosed paper IDS-A and PTO-1449 forms list Foreign Patent Documents and Other Documents cited in corresponding and other patent applications of the present named inventor; applicant encloses a copy of each listed reference.

Detailed Discussion of References Cited in Search Report Letters

Applicant relies upon the combination of all the limitations in the independent claims for patentability and not just the preceding general description.

Independent claims 25, 26, and 27 distinguish over the cited art by requiring: operating circuits; an expected data memory coupled to a serial data input lead; a comparator having first inputs coupled to the operating circuits and second inputs coupled to the expected data memory; a data register coupled to the first inputs of the comparator, to the serial data input lead, and to a serial data output lead; a mode select input lead; a serial data clock input lead; and an access port.

These elements are either formed on a substrate or are permanently integrated together.

Claims 25 and 26 further require a command register.

The following cited art fails to disclose an expected data memory coupled to a serial data input lead, and a data register coupled to the first inputs of a comparator and the serial data input and output leads, in the defined combinations.

Applicant could repeat a statement of these distinguishing limitations after the discussion of each following cited patent to meet the requirements of 37 CFR 1.111(b) and (c). Since each cited patent and the cited patents in combination fail to teach or suggest these distinguishing limitations, applicant will rely upon the preceding statement of the distinguishing limitations, without repetition.

US Patents

US 3,633,100 to Heilweil, et al., discloses applying two binary levels and an intermediate level of inputs to binary logic under test and to simulation logic. The outputs of the circuit under test and the simulation logic are compared to ascertain a good circuit.

US 3,651,315 to Collins discloses a digital inspection system. The outputs from a product under test are compared with the outputs of a known good unit.

US 3,657,527 to Kassabgi, et al., discloses a system for automatically checking boards bearing integrated circuits. A program card is read automatically to provide both test input signals to the board and simulation output signals representative of the correct output signals.

US 3,723,868 to Foster discloses digitally counting predetermined numbers of clock pulses during preselected timing intervals to determine the precise time interval between distinct edges of the output from a circuit under test and provide a GO/NO-GO indication.

US 4,433,413 to Fasang discloses a microprocessor system including a pseudo-random pattern generator, a signature register, supplemental control logic, serial and parallel I/O port test logic, and an LED display. Test instructions and the pattern generator provide test input data. The signature register and the microprocessor process the test results and present them on the display.

US 4,484,329 to Slamka, et al. discloses the jaw contacts of a clip 10 connecting a device under test to the external interface block 14 of a test device. Signals from the device under test are compared with signals output from a library block 20.

US 4,642,561 to Groves, et al., discloses compressing the amount of data stored in local test data RAMs for implementing a circuit test.

US 4,701,920 to Resnick, et al. discloses built-in self test circuitry 10 for LSI circuit chips. The test circuitry includes a serial scan path (TDI-TDO) and control signal logic 42. Input register 36 applies test signals to the main logic function 14 and output register 38 receives output signals from the main logic function 14.

US 4,701,921 to Powell, et al. discloses a modularized scan path for serially tested logic. Modules 26 each have serial registers 34-40, input gate 48 and output gate 50. Address 16 and control 12 leads connect to address decode/select 52, which selectively connects the scan data in leads 28 and the scan data out leads 30 to the modules for testing. Corresponds to US 4,710,931 and US 4,710,933.

US 4,710,933 to Powell, et al. discloses a parallel to serial scan system for testing logic circuits. Parallel registers 72-80 receive operational and test data from a common bus 70 and are selected by decoder 104. The test data passes through combinational logic and the responses are captured in serial register latches 92-102. Corresponds to US 4,701,921, and US 4,710,931.

US 4,857,835 to Whetsel appears not to be prior art to this application. This patent is to the same inventor as in this application and it issued on August 15, 1989. The present application claims priority to an application filed on June 30, 1989. In any event, IDS-A, Attachment A includes comments to this patent.

US 4,860,290 to Daniels, et al. discloses a logic circuit having individually testable logic modules. Each of the modules may be selected for testing by means of a scan path in the module made up of serial register latches (SRLs) 34. Each module has a test port 28a.

US 4,872,169 to Whetsel discloses a hierarchical scan selection system. A serial scan path can be compressed or expanded to pass only through the desired logic element(s) to be tested. Corresponds to JP 63-308,583.

US 4,893,072 to Matsumoto, et al., discloses testing an IC device 21 that includes a logic circuit section L and a memory circuit section M. Logic circuit section L includes flip-flops 30, 31, 32, and 33 that provide time delays between input and output signals through the IC 21. An IC-device testing apparatus 23 includes flip-flop circuits F11, F21, F22, ..., Fn, that provide for matching the time delays through the logic circuit section L of actual test signals applied to the IC 21 and expected signals EX. The IC tester applies a test signal to an IC under test and an expected response signal to the input of a shift register. The shift register is clocked to produce the expected response signal at its output at the same time the IC should produce its response

to the test signal. The tester then compares the expected response signal to the actual response signal.

US 4,947,357 to Stewart, et al. discloses a circuit board carrying plural integrated circuits, each with an internal scan chain. The scan input of each integrated circuit is connected to a system scan controller 26. The scan outputs of the integrated circuits are connected to multiplexer 30 for selective testing of individual integrated circuits.

US 5,001,713 to Whetsel appears not to be prior art to this application. This patent is to the same inventor as in this application and it issued on March 19, 1991. The present application claims priority to an application filed on June 30, 1989. In any event, IDS-A, Attachment A includes comments to this patent.

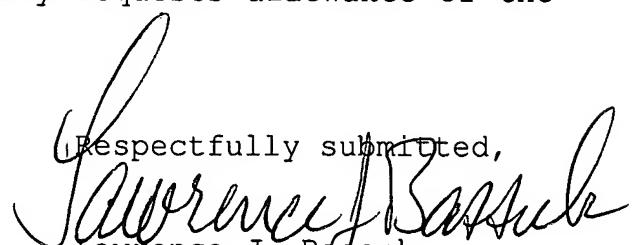
US 5,051,996 to Bergeson, et al. discloses a built-in test by signature system that provides fault detection by the bits in the signature detection logic.

US 5,077,740 to Kanuma discloses testing individual macrocells of a logic circuit by shifting test data into register 12, shutting off an input path for normal operation signals to the macrocell, and applying the test data in register 12 to the macrocell. An output register 14 receives the output of the macrocell under test and the contents of register 14 is shifted out, while shutting off an output path of normal operating signals from the macrocell.

US 5,090,015 to Dabbish, et al. discloses a self checking electronically erasable programmable array logic. The device verifies the storage integrity of each cell within the array during programming, after completing programming, and prior to executing the algorithm stored in the array.

Conclusion

The cited references, alone or in combination, fail to teach or suggest the claimed inventions. The application is in allowable form. Applicant respectfully requests allowance of the application.


Respectfully submitted,
Lawrence J. Bassuk
Reg. No. 29,043
Attorney for Applicant

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September 22, 2003

VIA FEDEX

Frank D. Cimino, Esq.
TEXAS INSTRUMENTS
 7839 Churchill Way
 Mail Station 3999
 Dallas, TX 75251

RE: JTAG & EXPECTED DATA CLAIM SET

Your Ref. No.: T14124D.X

Our Docket/Invoice No.: 30893.TI

Dear Frank:

In response to your letter dated September 11, 2003, we performed the patentability search, which you requested. The following is a complete report of our search parameters and findings.

SUBJECT MATTER OF SEARCH

In our search, we looked for specific limitations in concert with those embodied by the claims of your submitted disclosure. In particular, we searched for an integrated circuit that comprises of a substrate, operating circuits, a serial data input lead, a serial data output lead, an expected data memory, a comparator, a command register, a data register, a mode select input lead, a serial data clock input lead and access port, all formed on the substrate. Note that our search was limited to finding relevant US patents and foreign publications prior to June 30, 1989.

REFERENCES DISCOVERED

5,001,713	Whetsel
4,433,413	Fasang
4,701,920	Resnick et al.
4,893,072	Matsumoto
5,090,015	Dabbish et al.
5,077,740	Kanuma

Frank D. Cimino, Esq.
September 22, 2003
Page 2

5,051,996	Bergeson et al.
4,947,357	Stewart et al.
4,872,169	Whetsel, Jr.
4,857,835	Whetsel, Jr.
4,860,290	Daniels et al.
4,857,835	Whetsel, Jr.
4,710,933	Powell et al.
4,701,921	Powell et al.
4,642,561	Groves et al.
4,484,329	Slamka et al.
3,723,868	Foster
3,657,527	Kassabgi et al.
3,651,315	Collins
3,633,100	Hellwell et al.

DISCUSSION OF REFERENCES

Whetsel discloses an event qualified testing architecture for integrated circuits, which includes input circuitry, output circuitry, application logic circuitry and test circuitry (See Figures and Claims).

Fasang discloses a built-in apparatus and method for testing a microprocessor system, which includes memory means, data source means, signature register means and comparator means (See Figures and Claim 1).

Resnick et al. disclose a built-in self-test system for VLSI circuit chips, which includes test data input means, clock input means and shift register means (See Claims).

Matsumoto discloses apparatus for testing an integrated circuit device, which includes means for generating a test signal, means for generating an expected signal and means for comparing output with the expected signal (See Figures and Claims 1, 9 and 11).

The remaining references are cited as of general interest for your review.

Frank D. Cimino, Esq.
September 22, 2003
Page 3

FIELD OF SEARCH

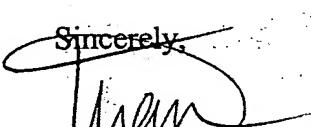
<u>CLASS</u>	<u>SUBCLASS</u>
714	25, 26, 27, 30, 31, 44, 724, 726, 727, 729, 730, 731, 733, 734, 736, 744, For. 100, For. 293, For. 300

In addition to a complete search of the above subclasses, Primary Examiner Stephen Baker of Group 2100 was consulted. This Examiner confirmed our opinion that the most pertinent search areas were covered by the above subclasses.

Enclosed are copies of the cited references and our invoice for services rendered and disbursements for this matter.

In closing; we would like to thank-you for giving us this opportunity to serve you.. If there are any questions or comments concerning this search or our services, please contact us at your earliest convenience.

Sincerely,


Tuan Nguyen